UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Electrical and Computer Engineering

EXPERIMENT 7 – PHASE LOCKED LOOPS

OBJECTIVES

The purpose of this lab is to familiarize students with the operation and application of a phase locked loop.

INTRODUCTION

A phase locked loop is a controlled oscillator whose instantaneous frequency is adjusted through multiplicative feedback and low pass filtering. The simplified PLL configuration used for analysis is shown in Figure 7-1 below. The three fundamental components are as follows: the voltage controlled oscillator (VCO), the phase detector (PD), and the loop filter (G(s)) with amplifier (A).

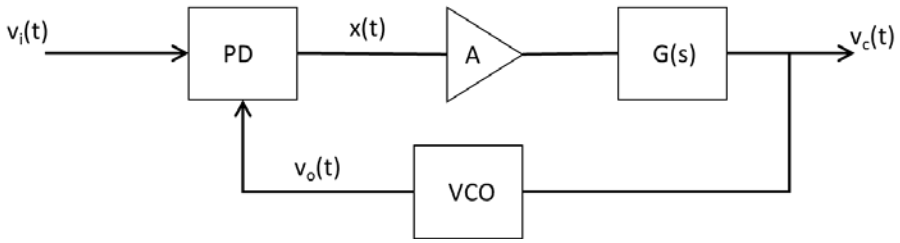

Figure 7-1 Simplified PLL Model

The voltage controlled oscillator is an oscillator whose instantaneous frequency $\omega_o(t)$ is controlled by the control voltage $v_c(t)$ according to the following equation:

$$\omega_o(t) = \omega_c + K_c v_c(t) \tag{1}$$

The waveform produced by the VCO can be a square wave, a sine wave, or one of many periodic waveforms. For the LM565 PLL, the waveform produced is sinusoidal. The constant ω_c is called the center frequency of the VCO. Note that, from the equation above, this is the free running frequency of the VCO when the control voltage v_c is equal to zero. The constant, K_c, is the VCO gain. It is a measure of the sensitivity of the VCO frequency variations to the control voltage. For the LM565 PLL, the VCO center frequency can be tuned through the selection of external components. In this experiment, these will be R_1 and C_1 connected to pins 8 and 9, respectively. For this configuration, the center frequency can be found from:

$$\omega_c = \frac{1.2\pi}{2R_1C_1} \tag{2}$$

The phase detector (PD) is a two-input one-output circuit operating according to the following characteristic. If the two inputs are periodic and have the same period, then the DC component

of the PD output should be approximately proportional to the phase angle between the two periodic inputs. This can be seen from the following equation:

$$x_{DC} = K_d \sin\left(\theta_i - \theta_o\right) \tag{3}$$

where x_{DC} is the average value (DC value) of the PD output. Similarly, θ_i represents the phase of the input signal, $v_i(t)$, and θ_o represents the phase of the VCO output signal, $v_o(t)$. The constant, K_d, is the phase detector gain. It is a measure of the sensitivity of the PD to output variations in the phase angle between the inputs. In general, the PD gain will depend upon the amplitude and the shape of the two periodic inputs, $v_i(t)$ and $v_o(t)$, to the PD. The size and shape of $v_o(t)$ is typically constant.

However, the input signal, $v_i(t)$, may vary in amplitude. If the amplitude of $v_i(t)$ is 200mV peak-to-peak or more K_d is constant and equal to approximately $1.4/\pi$ volts/rad. When the phase angle between the input is small, x_{DC} is a linear function of the phase angle since $\sin(\theta_i-\theta_o)$ is approximately equal to $(\theta_i-\theta_o)$ under these conditions.

The loop filter (including the amplifier) is the third fundamental component of the PLL. The filter is usually composed of external components. Completing the filter this way allows the PLL to be tunable. The loop filter is typically a passive low pass filter such as an RC filter. In this case, the voltage ratio transfer function G(s) is given by:

$$G(s) = \frac{1}{(1+\tau s)} = \frac{1}{(1+R_2C_2 s)} \tag{4}$$

The function of the loop filter is to extract the DC component of the PD output. Since the PD acts as a mixer, it's output will typically be periodic and will contain frequencies corresponding to the sums and differences of the frequencies present in $v_i(t)$ and $v_o(t)$. Thus, the 3dB cutoff frequency of the low pass filter should be considerably lower than $2\omega_i$ so that the filter output has low ripple when in phase lock.

When the PLL is in phase lock, the input frequency f_i equals the output frequency f_o. The filter output voltage is constant during this condition. If the input frequency increases slightly, the phase angle difference $\theta_i-\theta_o$ will increase in time. From equation (3), the DC output of the phase detector will increase, and then the DC output of the filter will increase. This will cause an increase to the input of the VCO, therefore increasing the VCO output frequency and bringing it up to meet the input frequency. The phase angle stabilizes at a new equilibrium, and phase lock is maintained. The new value of $\theta_i-\theta_o$ yields a larger constant output from the phase detector, which in turn drives the VCO at a higher frequency (further from the center frequency). A similar adjustment takes place when the input frequency is slightly less than the VCO frequency. In phase lock, this control circuit (PD, amplifier, and filter) is continuously adjusting the VCO frequency to equal the input frequency. The ability to maintain phase lock is governed by Equation (3). To maintain stability, the VCO frequency must increase when $\theta_i-\theta_o$ increases. However, from Equation (3), this will happen only when $\theta_i-\theta_o$ is greater than 0° and less than 90° or greater than 180° and less than 270°.

The capture range specifies the frequency limit beyond which a locked loop will become unlocked. The phase locked loop not only captures the specified frequency, but also captures the harmonic frequencies associated with the specified frequency. As the VCO output for this particular integrated circuit is rich in harmonics, additional capture ranges can be expected. The capture range for the LM565 PLL can be found from the following equation:

$$f_{capture} = \pm \frac{8 f_c}{V_c} \tag{5}$$

where fc is the center frequency and Vc is the total supply voltage.

This range of frequency is where the PLL will remain in lock with the input frequency once the PLL has locked initially. It is important to note that V_C is the total amount of supply voltage from both supply rails, e.g. $V_{dd} + |V_{ss}|$. The lock range of the PLL is the region where the PLL will phase lock to the input frequency, i.e. where the phase angle between the input and output is less than or equal to 45°. This region can be found from the equation below:

$$f_{lock} = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_{capture}}{\tau}} = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_{capture}}{(3.6k\Omega) C_2}} \quad \text{Note: } 3.6k\Omega \text{ is the internal to the PLL} \tag{6}$$

PRELAB

1. For the circuit shown in Figure 7-2, given R_1=4.3kΩ, calculate the value C_1 which yields a VCO center frequency of f_c = 5kHz.

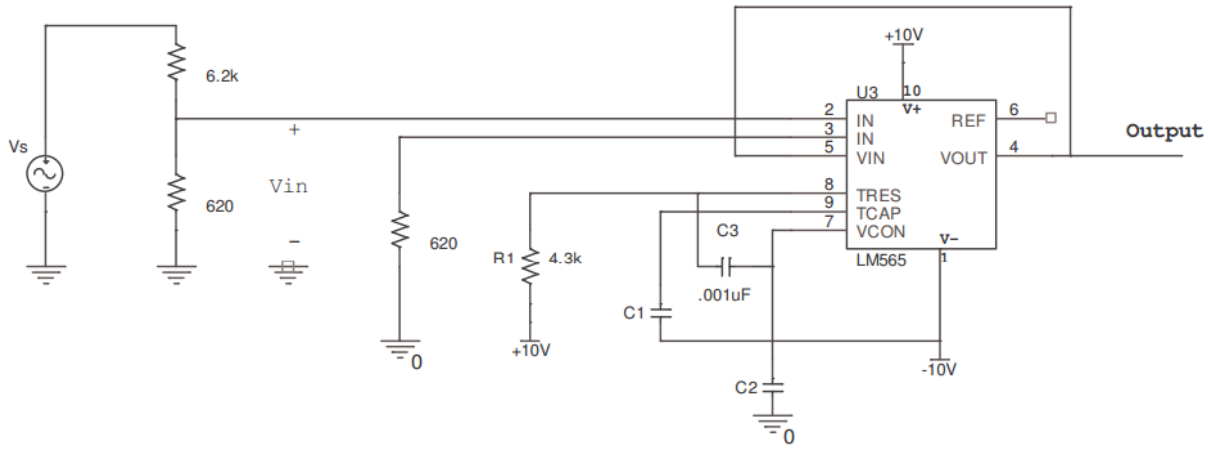

Figure 7-2 PLL Connection Diagram

2. Calculate the value for the theoretical capture range of the PLL given the supply voltages shown in Figure 7-2.
3. Calculate the value for C_2 which yields a lock range of ±1kHz.

PROCEDURE

1. Prepare the positive power supply to ensure a DC voltage of +10V.
2. Prepare the negative power supply to ensure a DC voltage of –10V.
3. Connect the circuit shown in Figure 7-2 using short leads and a compact physical layout to ensure that stray capacitance does not greatly affect the experiment.
4. Twist the power supply leads together also to reduce noise.
5. For C_1, use a decade capacitance box and for C_2, use your Prelab calculated value.
6. Adjust the function generator so that the input voltage V_{in} is a 200mV peak- to-peak sine wave.
7. Display the input voltage on Channel 1 and the output from the VCO (Pin 4) on Channel 2 of the oscilloscope.
8. Adjust the decade capacitor C_1 until the oscilloscope shows the output frequency to be 5kHz and the output signal is 90˚ out of phase with the input signal.
   a. To check this, make sure the output signal duty cycle is 50% and use the oscilloscope to measure the phase between channels 1 and 2. Record the value of C_1.
9. Vary the frequency of the function generator about the center frequency of 5kHz. Measure and record the lock range of the PLL.
   a. This can be measured finding the points at which the output signal is -90˚(+/-)45˚ out of phase with the input signal.
10. Now adjust the function generator to attain an input voltage V_{in} of 100mV peak-to-peak. Again measure and record the lock range of the PLL.
11. Readjust the output of the function generator to a voltage of 200mV peak-to- peak. Vary the frequency of the function generator about the center frequency of 5kHz, and this time vary it farther than when measuring the lock range.
    a. Measure and record the capture range of the PLL.
    b. This will occur when the output signal is no longer the same frequency as the input signal and the phase difference is -90˚(+/-)90˚.
12. Repeat step 11 with an input signal V_{in} of amplitude 100mV peak-to-peak and record the results.
13. This part of the experiment will investigate the use of the PLL as a frequency divider.
    a. Using a 200mV peak-to-peak sine wave for V_{in} measure the lock ranges when the input frequency is three times and five times the VCO frequency (i.e., f_{in} = 15kHz and 25kHz). Record the results.
    b. Vary the input frequency to two times and four times the VCO frequency (i.e., f_{in} =10kHz and 20kHz). Observe what takes place at the output of the VCO.

POST-LAB

Post-Lab questions must be answered in each experiment's laboratory report.

1. How well did the calculated lock range agree with the measured lock range obtained in Step 9 of the procedure? Did the lock range change significantly when reducing the input signal from 200mV to 100mV peak-to-peak in Step 10?
2. How well did the calculated capture range agree with the measured capture range obtained in Step 11 of the procedure? Was the capture range noticeably different with the reduced signal amplitude in Step 12?
3. When utilizing the PLL as a frequency divider why was there no (significant) lock range at even multiples of the center frequency of the VCO?

Be sure to include all items from the post-lab exercise above in your written lab report.