UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Electrical and Computer Engineering

EXPERIMENT 4 – COUNTING CIRCUITS

OBJECTIVES
In this laboratory the methods of sequential machine design will be explored by designing and building of a synchronous three-bit binary counter with a parallel load.

MATERIALS/EQUIPMENT NEEDED
DC Voltage Source (capable of 10 Vdc)
(2) SN7478 (JK Flip Flop)
(1) 7408 Quad 2-Input AND Gates
(2) 7400 Quad 2-Input NAND Gates
(1) 7404 Hex Inverters
4-bit Dip Switch
Micro Switch
(4) Resistor: 1 kΩ
(3) Resistor: 1.2 kΩ
(2) Resistor: 10 kΩ

INTRODUCTION
One of the more fundamental and important topics in digital circuits is that of counting and frequency division. Digital counters also function as frequency dividers with the clock frequency out of the least significant bit being one-half that of the input clock, the output of the next least significant bit being one-half that of the least significant output and on down to the output frequency of the most significant bit which is $f_i/2^n$. The size of a digital counter is measured in bits (n) and can count up to a binary number of 2^n. Counters of size n = 28 and larger are available in integrated circuit packages, so in most cases it is not necessary to design and build counters the old fashion way, with a string of flip-flops and combinational logic.

Nevertheless, the methods used to design counters are those used to design digital sequential machines in general and should be familiar topics to all students in electronics. In some cases a non-sequential counting sequence is desired and in others it may be desirable to use a divided frequency that is not an output on an available integrated circuit counter. Under these circumstance a simple counter design using D, T or J-K flip-flops may be desirable. Also, in order to obtain laboratory results without waiting for an integrated circuit to be ordered, a small counter can be built in a short time with minimal trouble.

PRELAB

1. Design and draw the schematic diagram for a three-bit binary counter. The counter must have a pulsed parallel load with a pulse input L_d and parallel data inputs A, B, and C. The logic circuit needed for the parallel load, separate from the feedback logic, will load the desired initial state when the L_d pulse is applied. This logic circuit provides the parallel load via the active-low asynchronous Preset and Clear inputs to the flip-flops. Three T flip-flops will be used for memory and the feedback logic plus parallel load logic will be provided with the appropriate combination of NAND-gates, AND-gates, and Inverters. The T flip-flops will be implemented with J-K flip-flops that have their J and K inputs tied together. For this counter the total input for the sequential machine is simply the present state (QA, QB, QC). Consequentially, there will be three independent variables in the feedback logic design. The outputs of the feedback logic will be the excitation (TA, TB, TC). The outputs for the sequential machine will be the flip-flop outputs or the present state. Sequential machines where the outputs are a function of the present state only are known as Moore machines. Refer to Figure 4-1 to see the required external connections for this counter. Be sure to present all steps of your design with a neat and clear diagram of the required circuit.

Note: The required design procedure is discussed in numerous introductory text books on sequential machine design and will not be repeated here. However, the essential steps for such a design will include in order: the development of a Flow Diagram, the development of a State Transition Table, the development of an Excitation Table, and finally the design of the feedback logic using Karnaugh maps or an equivalent logic reduction method.

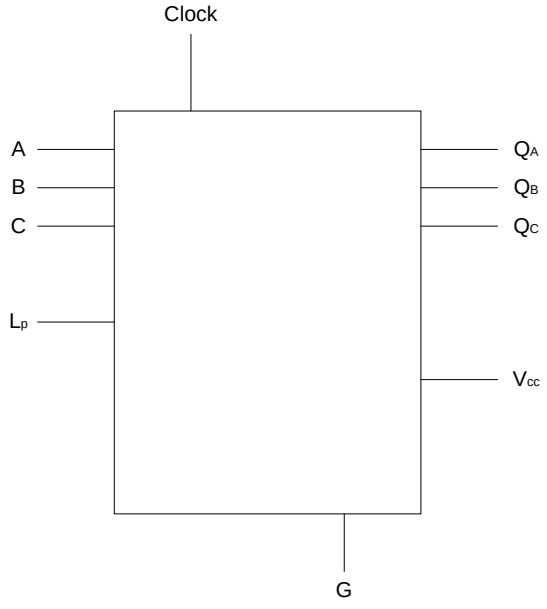

Figure 4-1 Block diagram for a digital counter showing the required external connections

2. Simulate your synchronous three-bit binary counter with a parallel load in Multisim or Pspice to verify you obtain the desired results.

PROCEDURE

1. Construct the circuit designed in part 1 of the Pre-Lab.
2. Use LED's to monitor the counter outputs, and slide switches to provide the parallel inputs and loading pulse. Each LED will need to be in series with a 1.2 kΩ current limiting resistor.
3. Use the switch debouncing circuit used in Experiment #2 to provide the clock signal. This will allow you to observe changes in the output with each trailing edge of the clock.
4. Demonstrate the operation of your counter to the lab TA before leaving the lab.

INSTRUCTOR'S INITIALS: | DATE:

POST-LAB

1. Develop the State Transition Table for a 3-bit counter that will count in the sequence 000, 010, 001, 100, 011, 110, 111, 101, 000

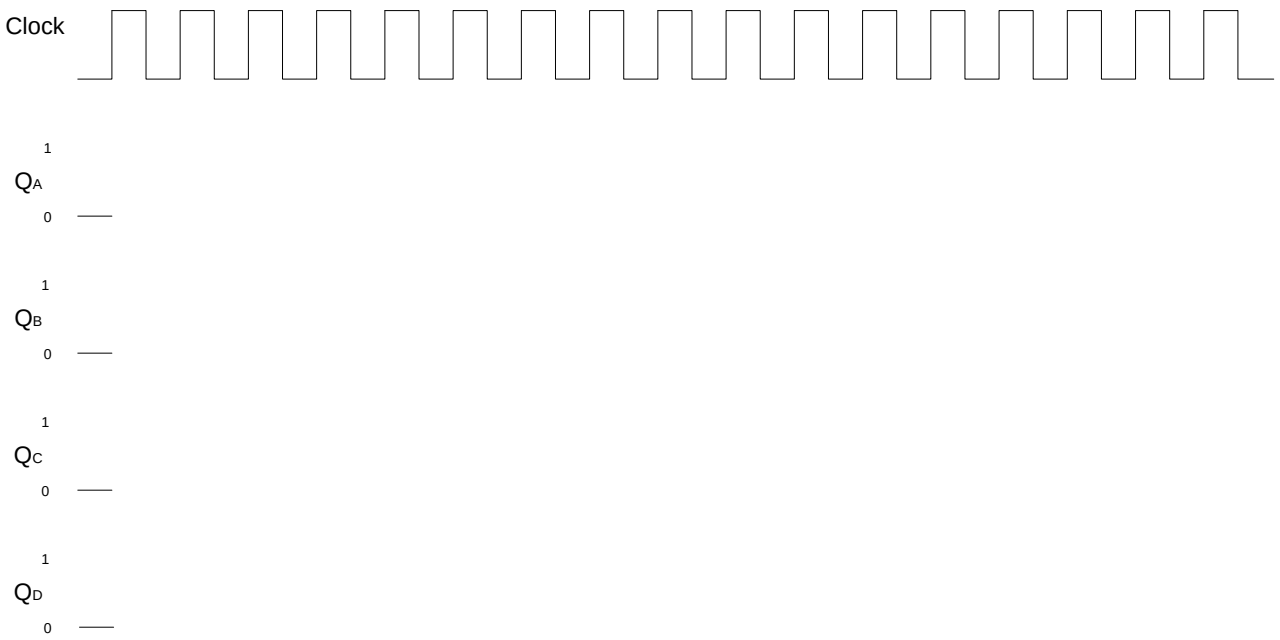

Figure 4-2 Timing Diagram for part #1 of Post-Lab

2. Provide a list of problems encountered and how they were resolved.

Be sure to include all items from the post-lab exercise above in your written lab report.