UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Electrical and Computer Engineering

EXPERIMENT 3 – SEVEN SEGMENT DECODER

OBJECTIVES
The student will learn how to implement a digital design in a testable model using a breadboard and logic. During this experiment students should acquire the basic skills needed to take a simple design description to a working and testable version.

MATERIALS/EQUIPMENT NEEDED
DC Voltage Source (capable of 10 Vdc)
(1) four-bit dip switch
(1) 7447 (BCD to seven-segment decoder driver)
(7) 470 Ω - current limiting resistors
(4) 1kΩ – resistors
(1) Common anode seven segment display

INTRODUCTION
A seven-segment decoder is a logic circuit often used for the visual display of digital information. The seven outputs of the decoder will drive the seven segments on a corresponding display. BCD is the acronym for Binary Coded Decimal. The BCD system is used to represent the decimal numbers from 0 to 9 in a binary format suitable for digital devices. A four-bit code is required with the decimal characters 0 through 9 represented by the binary numbers 0000 through 1001. The combinations 1010 through 1111 are not used. A BCD to seven-segment decoder will allow the display of a binary coded decimal on a seven-segment display. The input to the decoder is a number from 0 through 9 in BCD and the output provides the seven inputs required to drive the seven-segment display.

In the early years of digital design such a logic circuit would have been implemented using SSI technology; however, for many years popular circuits such as the BCD to seven-segment decoder have been available in MSI packages. Although our design will include the development of logic circuits for the BCD to seven-segment decoder, to simplify our laboratory circuit, the 7447 (BCD to seven-segment decoder driver) will be used. Simple dipswitches will provide the BCD input to the 7447 and the output of which will drive the seven-segment display. The display controller for a BCD to seven-segment decoder/driver will be developed as indicated in Figure 3-1.

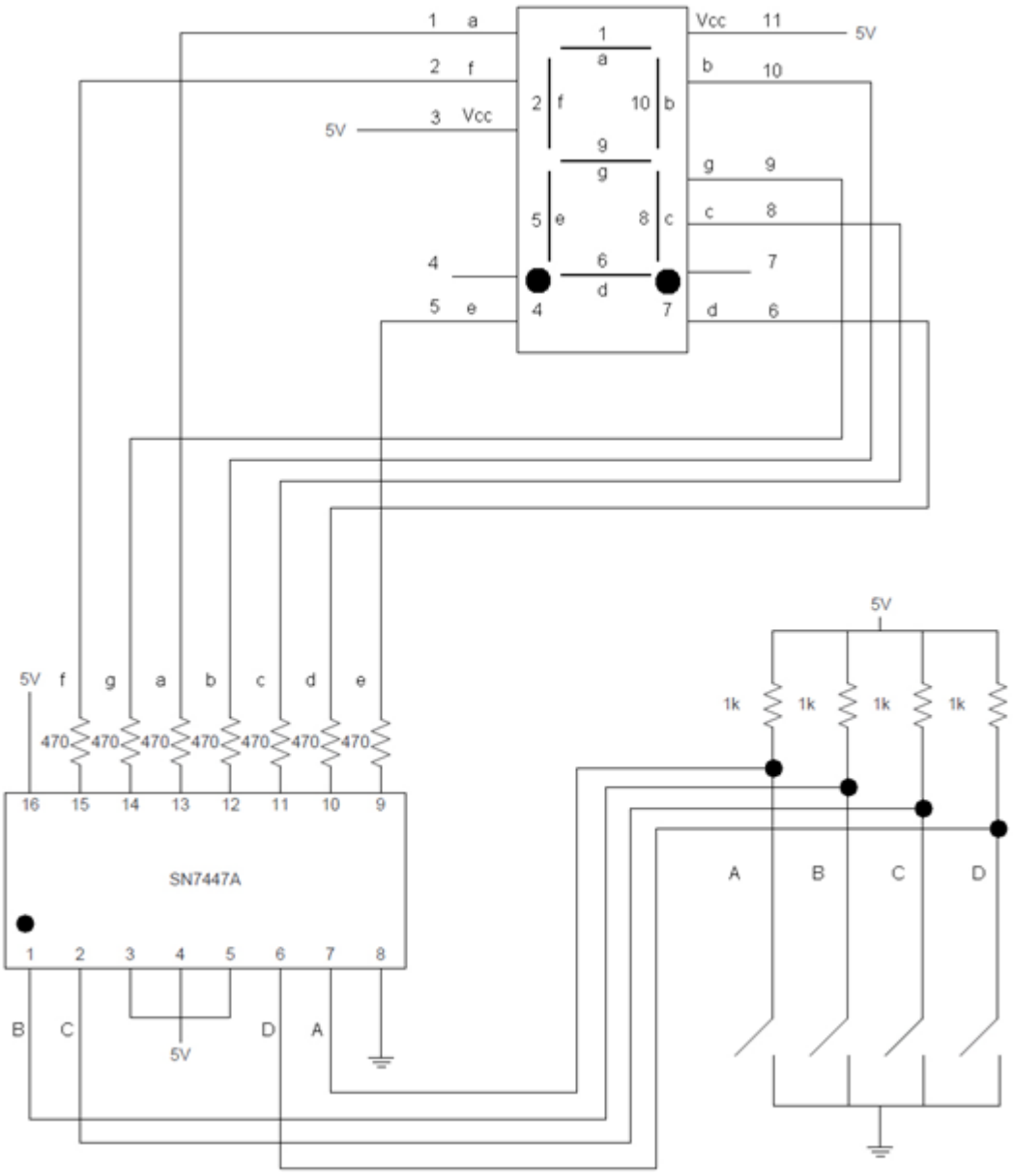

Figure 3-1 Circuit diagram for LED display

PRELAB

1. Create the truth table describing the function of a BCD to seven-segment decoder. The lower case letters, a-g, represent the segments on the display while the upper case letters A-D represent the BCD input. Observe that A is the lest-significant bit of the BCD input.

Table 3-1: Truth table for a BCD to seven-segment decoder

	BCD Inputs				Seven Segment Display (Outputs)						
#	D	C	B	A	a	b	c	d	e	f	g
0											
1											
2											
3											
4											
5											
6											
7											
8											
9											

2. After completing the truth table, make K-maps for each of the seven outputs. Reduce the K-maps to obtain a minimal sum of products expression for each segment.
3. For each K-map, draw the gate level circuits that the equation represents. **Note:** Use AND gates and OR gates as required for a two level implementation. Assume that inputs are available in complimented and un-complimented form
4. Simulate your circuits in Multisim or Pspice to verify you obtain the desired outputs.

PROCEDURE

As previously stated we will not implement the BCD to seven-segment decoder with SSI logic. Instead, as shown in Figure 3-1, the 7447 (BCD to seven-segment decoder driver) will be used. This circuit has a BCD input (DCBA) and seven outputs (abcdefg). The outputs of the 7447 are active low and must be used with a common anode LED display.

1. Construct the circuit of Figure 3-1.
2. The four-bit dipswitch will provide the input to the BCD to seven-segment decoder/driver. Remember that the maximum valid input is 9 (1001), record the outputs in Table 3-2.
3. Observe and document in Table 3-2 the outputs for inputs greater than 9.
4. Any errors should be traceable with a multimeter. Debugging if required should be documented for submission with your report.
5. Demonstrate the working display to the lab TA before leaving the lab.

DATA/OBSERVATIONS

Table 3-2: Output observed on seven segment display

Input	Output
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	

Input	Output
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

INSTRUCTOR'S INITIALS: DATE:

POST-LAB

1. Include in the report: all truth tables, k-maps, hand-written or computer drawn schematics from the Pre-Lab, and a schematic of the complete circuit design.
2. Provide a list of problems encountered and how they were resolved should be included.

Be sure to include all items from the post-lab exercise above in your written lab report.